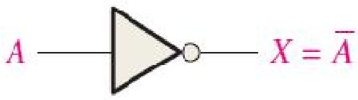
Logic Gates

3.1 The Inverter (NOT) Gate:

The inverter (NOT circuit) performs the operation called *inversion* or *complementation.* The inverter changes one logic level to the opposite level. In terms of bits, it changes a 1 to a 0 and a 0 to a 1. Standard logic symbols for the **inverter** are shown in Figure (3.1).



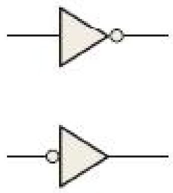


Figure (3.1): Standard logic symbols for the inverter.

The operation of an inverter (NOT circuit) can be expressed as follows: If the input variable is called ***A***and the output variable is called ***X***, then:

$$X = \overline{A}$$

This expression states that the output is the complement of the input, so if A = 0, then X = 1, and if A = 1, then X = 0.

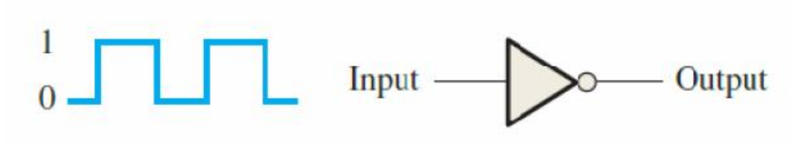
This operation is summarized in **Table (3.1),** a table such as this is called a **truth table.**

Table (3.1)

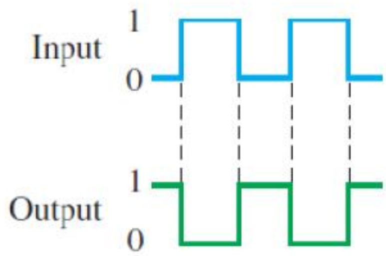
Inverter truth table.

Input	Output
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)

EXAMPLE 1: A waveform is applied to an inverter in Figure below. Determine the output waveformcorresponding to the input and show the timing diagram. According to the placement ofthe bubble, what is the active output state?



Solution: The output waveform is exactly opposite to the input (inverted), as shown in Figure below,which is the basic timing diagram. The active or asserted output state is **0**.



3.2 The AND Gate:

The AND gate can have two or more inputs and performs what is known as logical multiplication.

The operation of a 2-input AND gate can be expressed in equation form as follows: If one input variable is *A*, if the other input variable is *B*, and if the output variable is *X*, then the Boolean expression is:***X* = *A*.*B***

OR:* *X* = *AB

Figure (3.2) shows the AND gate logic symbol with two, three, and four input variables and the output variables indicated.

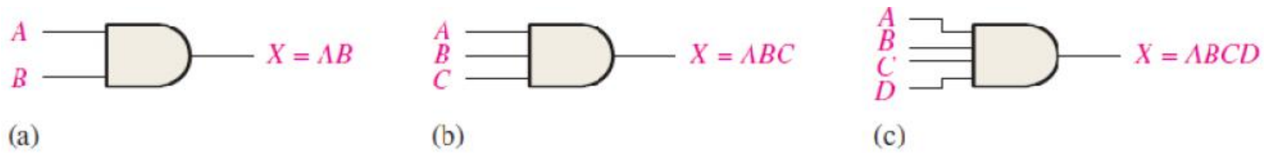


Figure (3.2): Boolean expressions for AND gates with two, three, and four inputs.

Figure (3.3) illustrates a 2-input AND gate with all four possibilities of input combinations and the resulting output for each.

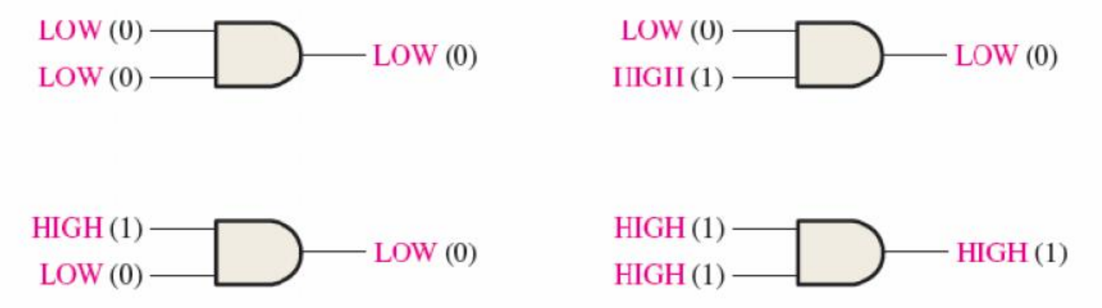


Figure (3.3): All possible logic levels for a 2-input AND gate.

The logical operation of a gate can be expressed with a truth table that lists all input combinations with the corresponding outputs, as illustrated in Table (3.2) for a 2-input AND gate.

Table (3.2): Truth table for a 2-input AND gate.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	0
1	0	0
1	1	1

1 = HIGH, 0 = LOW

The total number of possible combinations of binary inputs to a gate is determined by the following formula:

$$N = 2^n$$

where N is the number of possible input combinations and n is the number of input variables. To illustrate,

For two input variables: $N = 2^2 = 4$ combinations

For three input variables: $N = 2^3 = 8$ combinations

For four input variables: $N = 2^4 = 16$ combinations

EXAMPLE 2: (a) Develop the truth table for a 3-input AND gate.

(b) Determine the total number of possible input combinations for a 4-input AND gate.

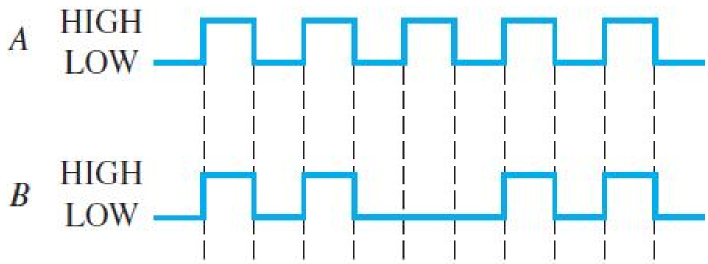
Solution:

(a) There are eight possible input combinations ($2^3 = 8$) for a 3-input AND gate. Theinput side of the truth table (Table below) shows all eight combinations of three bits.The output side is all 0s except when all three input bits are 1s.

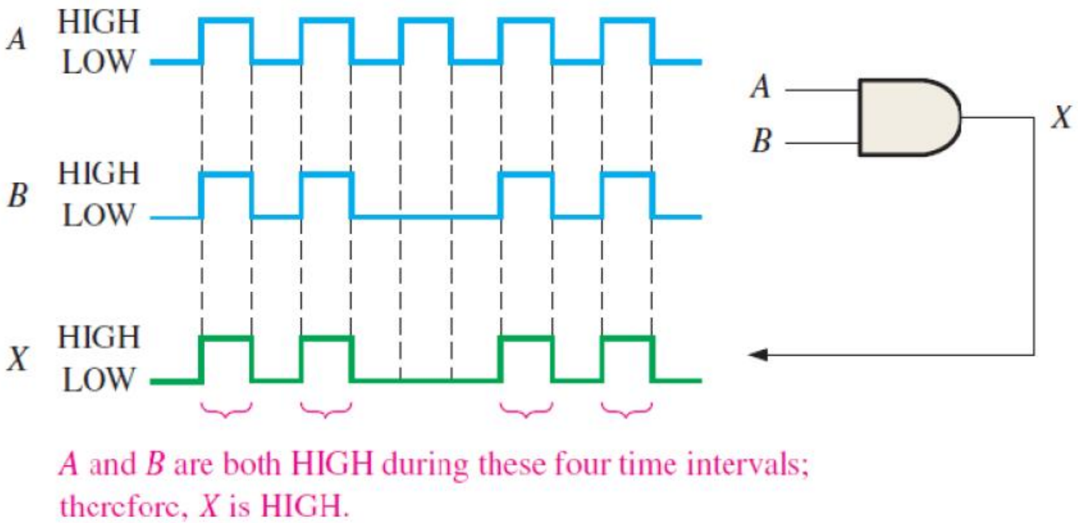
Inputs			Output
A	*B*	*C*	*X*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(b) $N = 2^4 =$ **16**. There are 16 possible combinations of input bits for a 4-input AND gate.

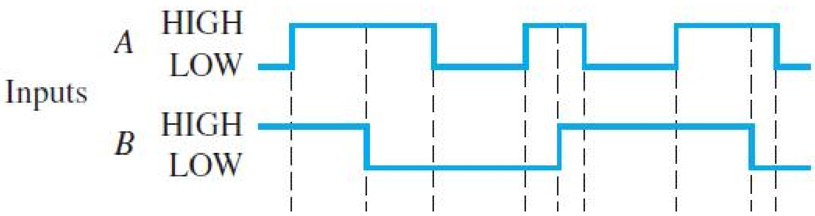
EXAMPLE 3: If two waveforms, *A* and *B*, are applied to the AND gate inputs as in Figure below, whatis the resulting output waveform?



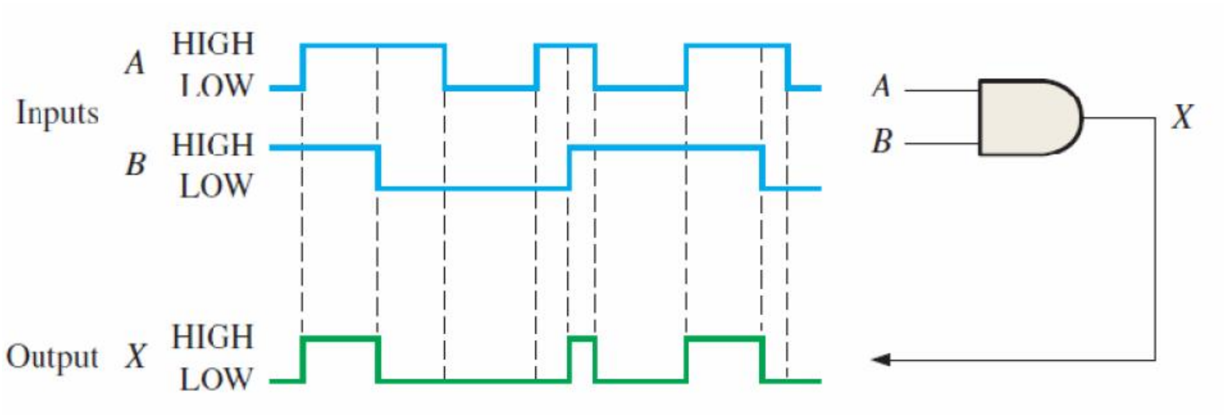
Solution: The output waveform *X* is HIGH only when both *A* and *B* waveforms are HIGH as shown in the timing diagram in Figure below.



EXAMPLE 4: For the two input waveforms, *A* and *B*, in Figure below, show the output waveform withits proper relation to the inputs.



Solution: The output waveform is HIGH only when both of the input waveforms are HIGH asshown in the timing diagram.



3.3 The OR Gate:

The OR gate can have two or more inputs and performs what is known as logical addition.

The operation of a 2-input OR gate can be expressed as follows: If one input variable is *A*, if the other input variable is *B*, and if the output variable is *X*, then the Boolean expression is:

$$X = A + B$$

The plus sign is read as “OR”.

Figure (3.4) shows the OR gate logic symbol with two, three, and four input variables and the output variables labeled.

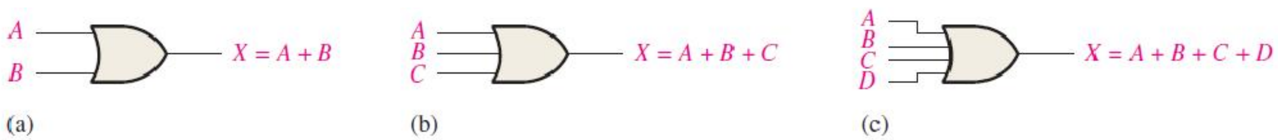


Figure (3.4): Boolean expressions for OR gates with two, three, and four inputs.

Figure (3.5) illustrates a 2-input OR gate for all four possibilities of input combinations.

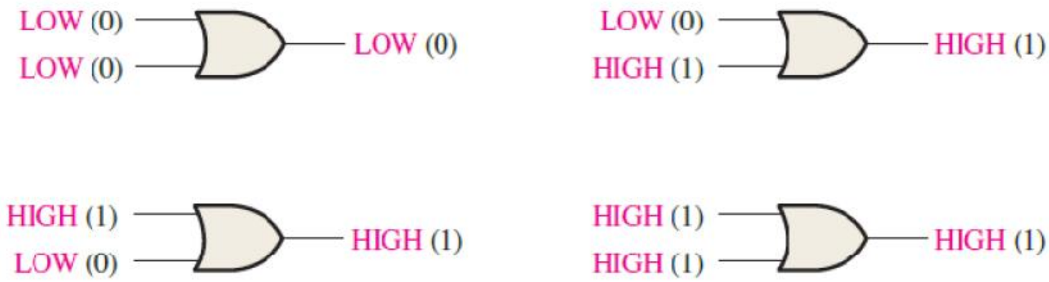


Figure (3.5): All possible logic levels for a 2-input OR gate.

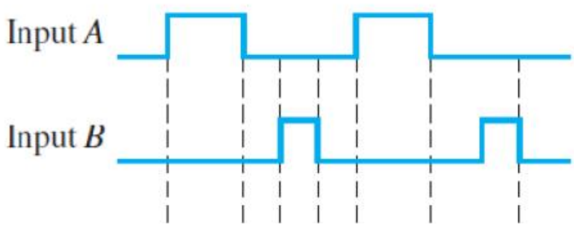
The operation of a 2-input OR gate is described in Table (3.3).

Table (3.3): Truth table for a 2-input OR gate.

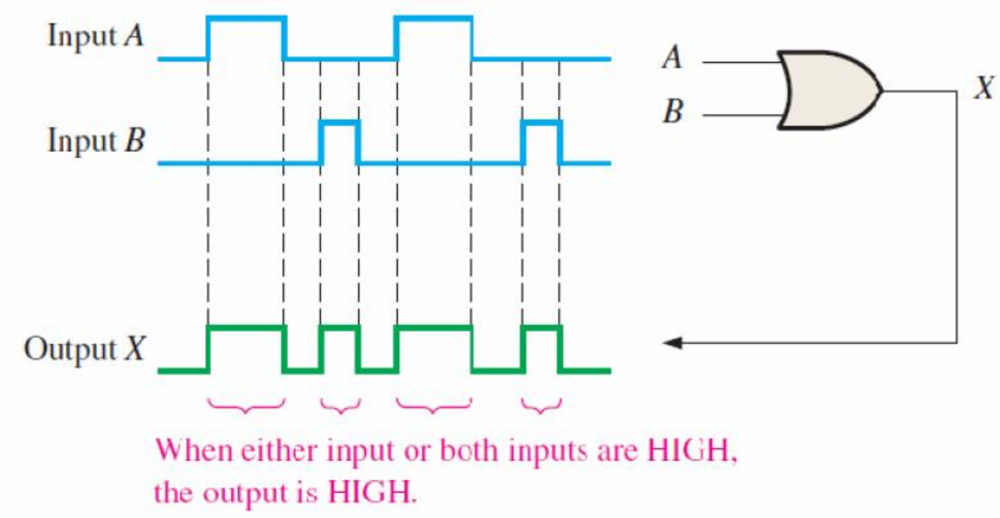
Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	1

1 = HIGH, 0 = LOW

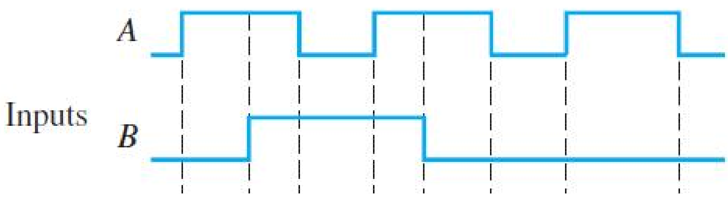
EXAMPLE 5: If the two input waveforms, *A* and *B*, in Figure below are applied to the OR gate, what isthe resulting output waveform?



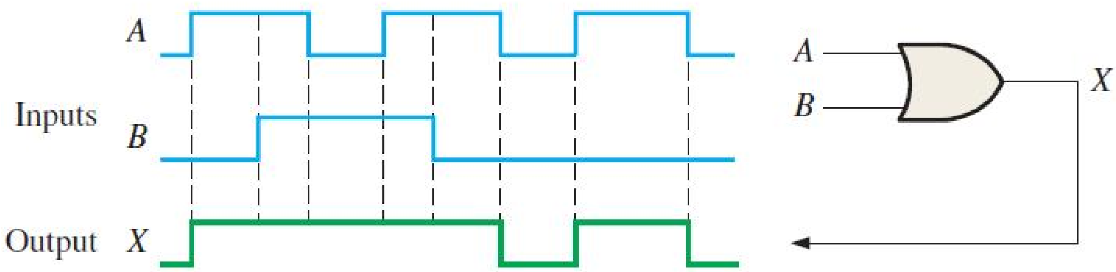
Solution: The output waveform *X* of a 2-input OR gate is HIGH when either or both input waveformsare HIGH as shown in the timing diagram. In this case, both input waveforms arenever HIGH at the same time.



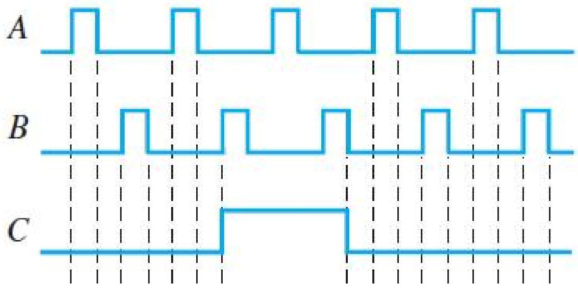
EXAMPLE 6: For the two input waveforms, *A* and *B*, in Figure below, show the output waveform withits proper relation to the inputs.



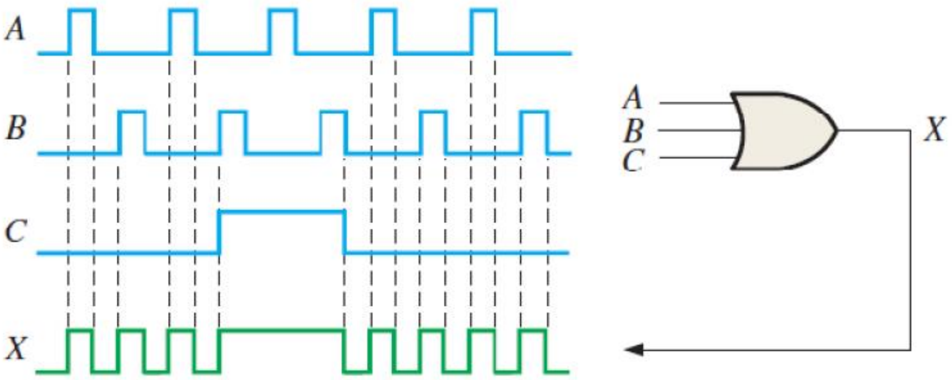
Solution: When either or both input waveforms are HIGH, the output is HIGH as shown by theoutput waveform *X* in the timing diagram.



EXAMPLE 7: For the 3-input OR gate in Figure below, determine the output waveform in proper timerelation to the inputs.



Solution: The output is HIGH when one or more of the input waveforms are HIGH as indicatedby the output waveform *X* in the timing diagram.



3.4 The NAND Gate:

The NAND gate is a popular logic element because it can be used as a universal gate; that is, NAND gates can be used in combination to perform the AND, OR, and inverter operations.

The term *NAND* is a contraction of NOT-AND and implies an AND function with a complemented (inverted) output. The standard logic symbol for a 2-input NAND gate and its equivalent are shown in Figure (3.6).

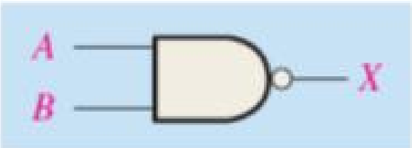


Figure (3.6): Standard NAND gate logic symbols

The Boolean expression for the output of a 2-input NAND gate is:

$$X = \overline{AB}$$

Figure (3.7) illustrates the operation of a 2-input NAND gate for all four input combinations, and Table (3.4) is the truth table summarizing the logical operation of the 2-input NAND gate.

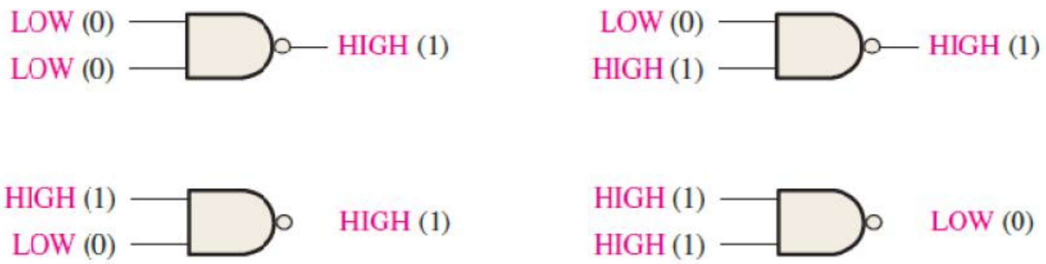


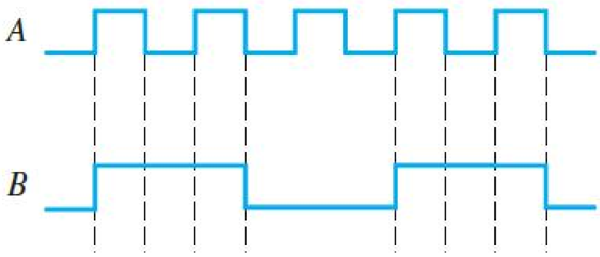
Figure (3.7): Operation of a 2-input NAND gate.

Table (3.4): Truth table for a 2-input NAND gate.

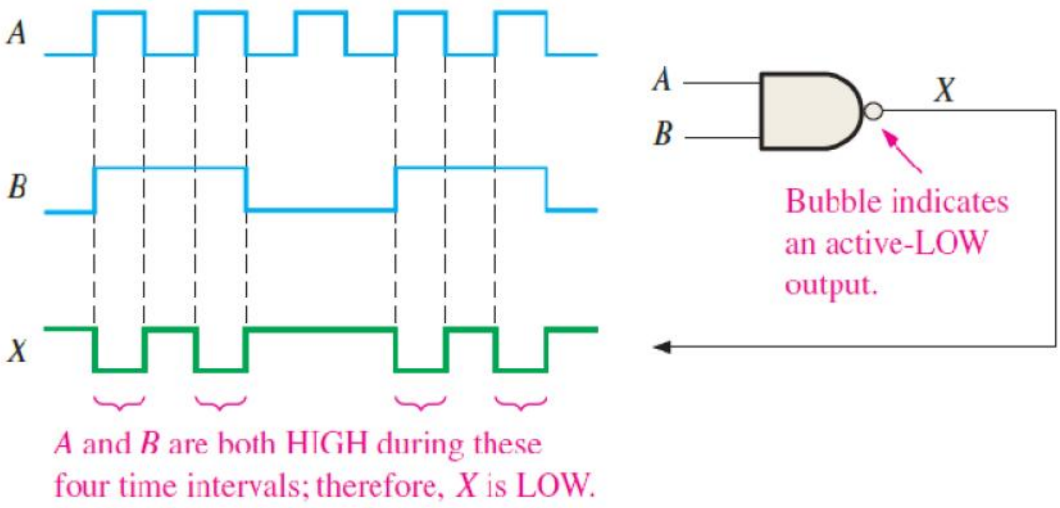
Inputs		Output
A	*B*	*X*
0	0	1
0	1	1
1	0	1
1	1	0

1 − HIGH, 0 − LOW.

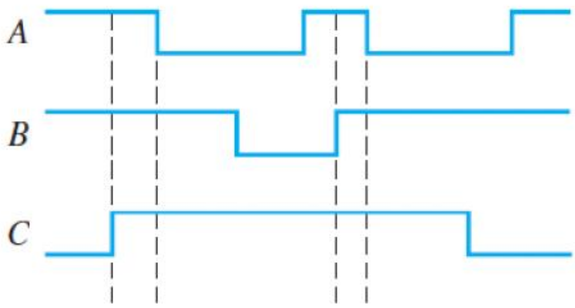
EXAMPLE 8: If the two waveforms *A* and *B* shown in Figure below are applied to the NAND gateinputs, determine the resulting output waveform.



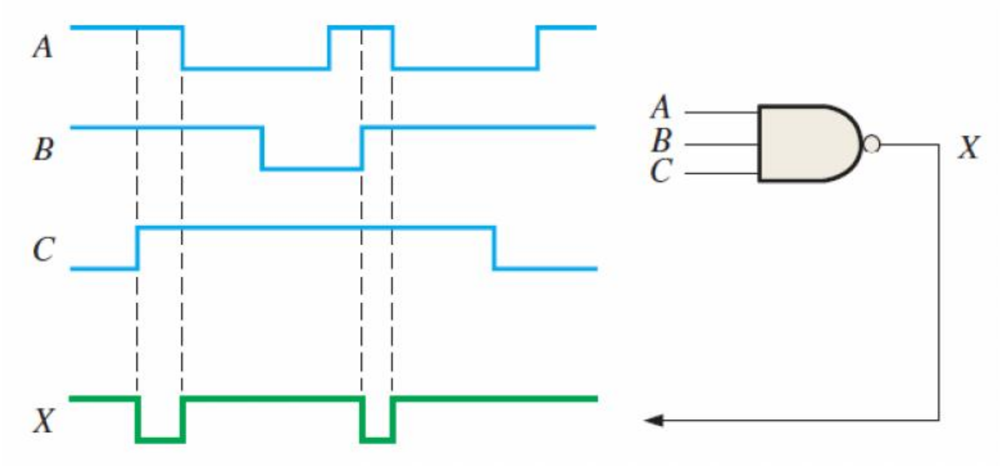
Solution: Output waveform *X* is LOW only during the four time intervals when both input waveforms*A* and *B* are HIGH as shown in the timing diagram.



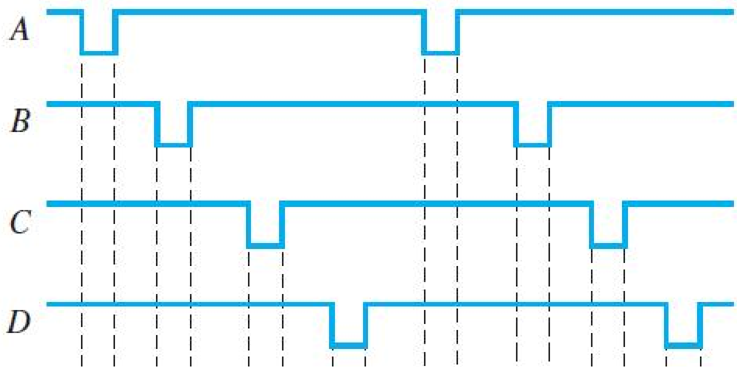
EXAMPLE 9: Show the output waveform for the 3-input NAND gate in Figure below with its propertime relationship to the inputs.



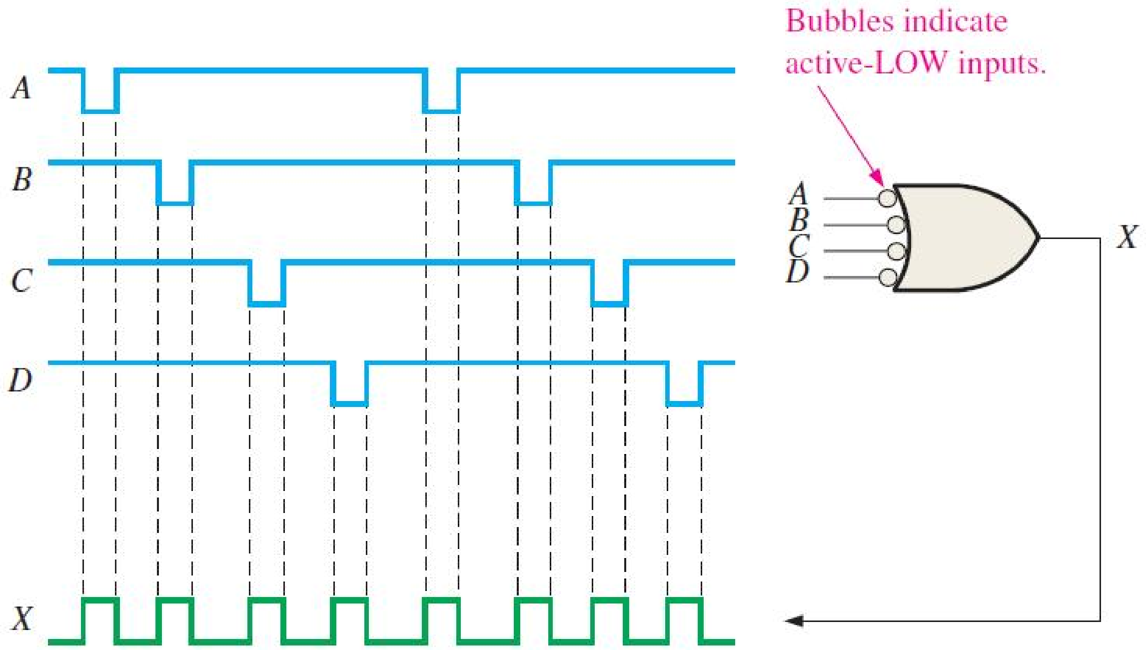
Solution: The output waveform *X* is LOW only when all three input waveforms are HIGH asshown in the timing diagram.



EXAMPLE 10: For the 4-input NAND gate in Figure below, operating as a negative-OR gate, determinethe output with respect to the inputs.



Solution: The output waveform *X* is HIGH any time an input waveform is LOW as shown in thetiming diagram.



3.5 The NOR Gate:

The NOR gate, like the NAND gate, is a useful logic element because it can also be used as a universal gate; that is, NOR gates can be used in combination to perform the AND, OR, and inverter operations.

The term *NOR* is a contraction of NOT-OR and implies an OR function with an inverted (complemented) output. The standard logic symbol for a 2-input NOR gate and its equivalent are shown in Figure (3.8).

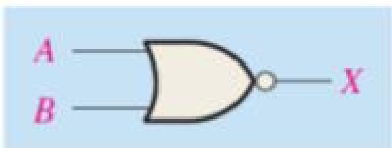


Figure (3.8): Standard NOR gate logic symbols.

The Boolean expression for the output of a 2-input NOR gate can be written as:

$$X = \overline{A + B}$$

Figure (3.9) illustrates the operation of a 2-input NOR gate for all four possible input combinations, and Table (3.5) is the truth table for a 2-input NOR gate.

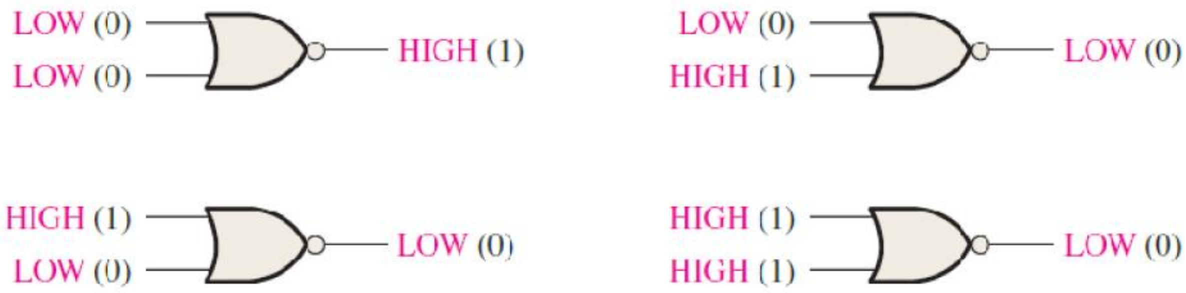


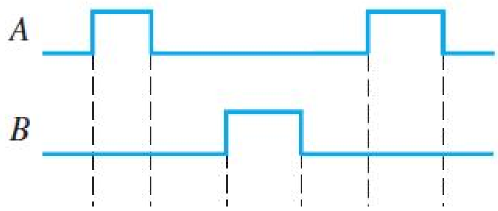
Figure (3.9): Operation of a 2-input NOR gate.

Table (3.5): Truth table for a 2-input NOR gate.

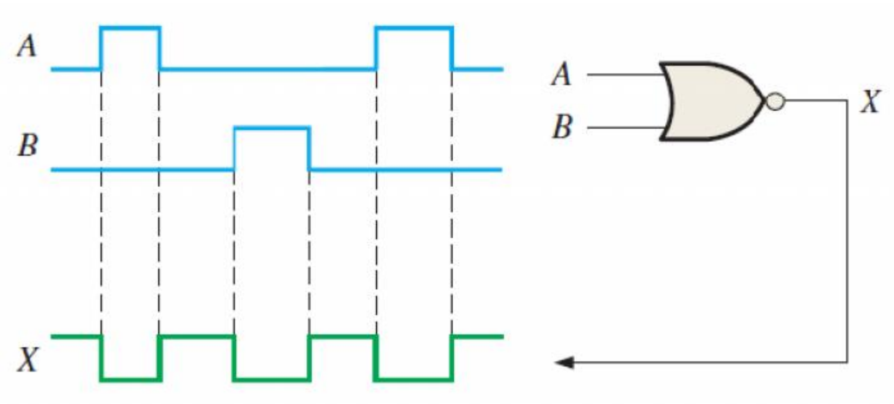
Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	0

1 = HIGH, 0 = LOW.

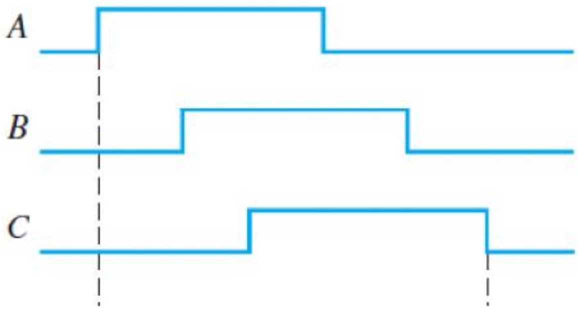
EXAMPLE 11: If the two waveforms shown in Figure below are applied to a NOR gate, what is theresulting output waveform?



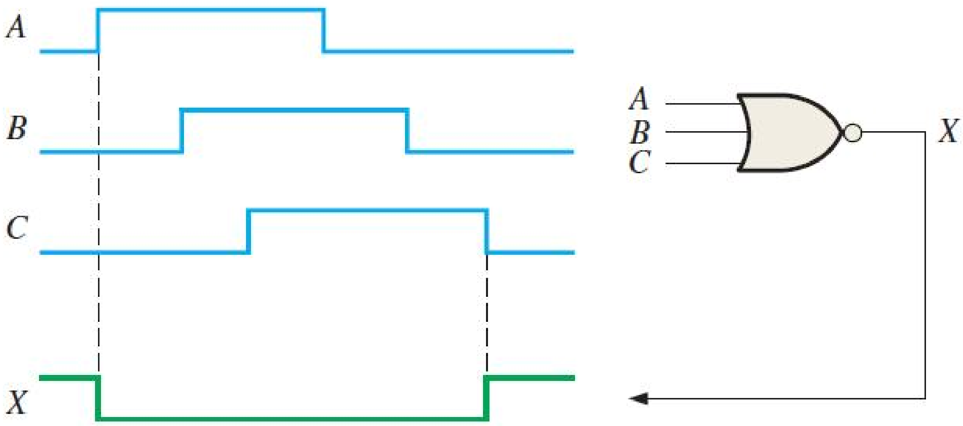
Solution: Whenever any input of the NOR gate is HIGH, the output is LOW as shown by theoutput waveform *X* in the timing diagram.



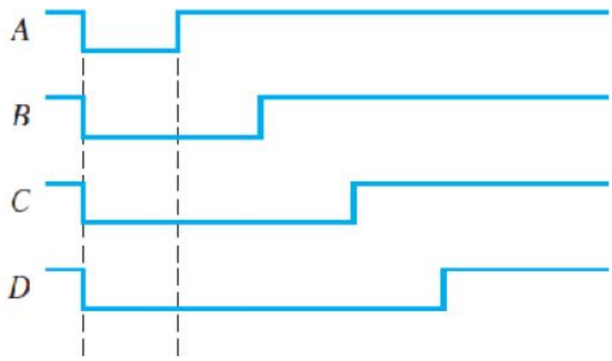
EXAMPLE 12: Show the output waveform for the 3-input NOR gate in Figure below with the propertime relation to the inputs.



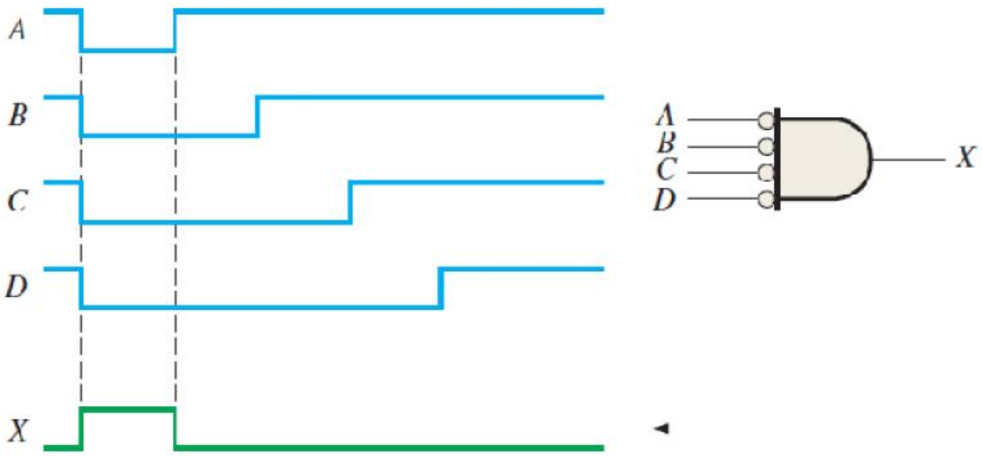
Solution: The output *X* is LOW when any input is HIGH as shown by the output waveform *X* inthe timing diagram.



EXAMPLE 13: For the 4-input NOR gate operating as a negative-AND in Figure below, determine theoutput relative to the inputs.



Solution: Any time all of the input waveforms are LOW, the output is HIGH as shown by outputwaveform *X* in the timing diagram.



3.6 The Exclusive-OR Gate:

The **exclusive-OR gate** performs modulo-2 addition.Standard symbols for an exclusive-OR (XOR for short) gate are shown in Figure (3.10).

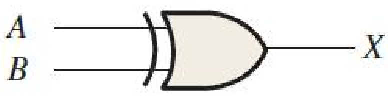


Figure (3.10): Standard logic symbols for the exclusive-OR gate.

The Boolean expression for the output of a 2-input XOR gate can be written as:

$$X=\overline{A}B + A\overline{B} = A \oplus B$$

The XOR gate has only two inputs.The four possible input combinations and the resulting outputs for an XOR gate are illustrated in Figure (3.11). The operation of an XOR gate is summarized in the truth table shown in Table (3.6).

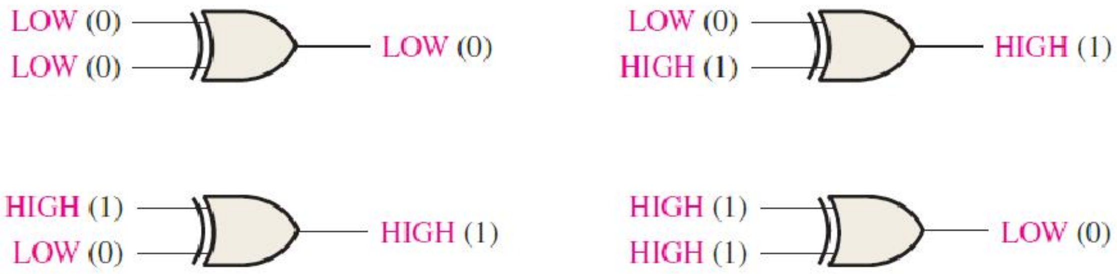


Figure (3.11): All possible logic levels for an exclusive-OR gate.

Table (3.6): Truth table for an exclusive-OR gate.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	0

3.7 The Exclusive-NOR Gate:

The bubble on the output of the XNOR symbolindicates that its output is opposite that of the XOR gate.Standard symbols for an **exclusive-NOR** (XNOR) **gate** are shown in Figure (6.12).

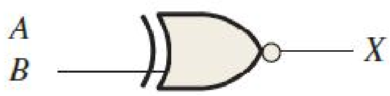


Figure (6.12): Standard logic symbols for the exclusive-NOR gate.

The Boolean expression for the output of a 2-input XNOR gate can be written as:

$$X = \overline{A}\overline{B} + AB = \overline{A \oplus B}$$

Like theXOR gate, an XNOR has only two inputs.The four possible input combinations and the resulting outputs for an XNOR gate areshown in Figure (3.13). The operation of an XNOR gate is summarized in Table (3.7).

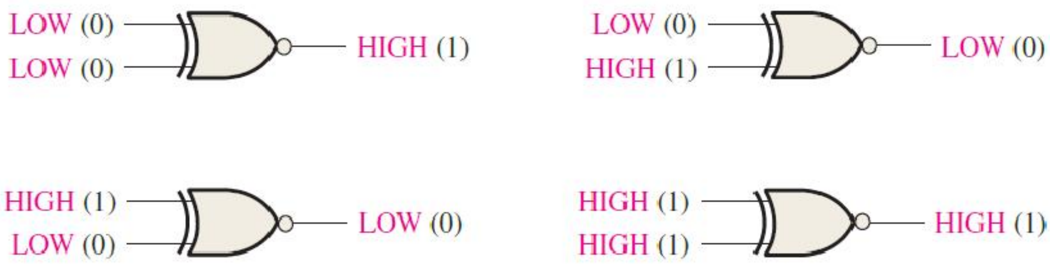
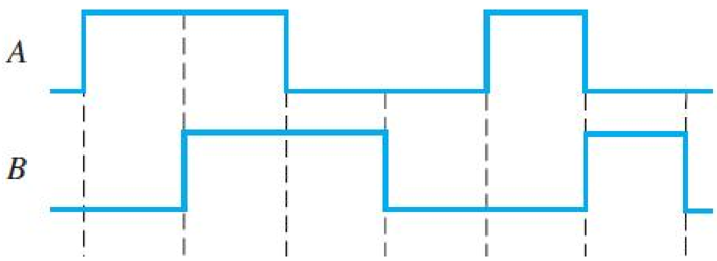


Figure (3.13): All possible logic levels for an exclusive-NOR gate.

Table (6.7): Truth table for an exclusive-NOR gate.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	1

EXAMPLE 14: Determine the output waveforms for the XOR gate and for the XNOR gate, given theinput waveforms, *A* and *B*, in Figure below.



Solution: The output waveforms are shown in Figure below. Notice that the XOR output is HIGHonly when both inputs are at opposite levels. Notice that the XNOR output is HIGHonly when both inputs are the same.